Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **PI-8**
2. **Q6**
3. **Q8**
4. **PI-4**
5. **PI-3**
6. **PI-2**
7. **PI-1**
8. **VSS**
9. **PARALLEL/SERIAL CONTROL**
10. **CLOCK**
11. **SERIAL IN**
12. **Q7**
13. **PI-5**
14. **PI-6**
15. **PI-7**
16. **VDD**

**.074”**

**3 2 1 16 15**

**MASK**

**REF**

**14**

**13**

**12**

**11**

**4**

**5**

**6**

**7 8 9 10**

**CD4014B**

**.084”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0033” X .0033”**

**Backside Potential: VDD**

**Mask Ref: CD4014B**

**APPROVED BY: DK DIE SIZE .074” X .084” DATE: 9/8/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD4014BH**

**DG 10.1.2**

#### Rev B, 7/19/02